Customer No.: 31561
Application No.: 10/065,345
Docket No.: 9069-US-PA

IN THE CLAIMS

Please amend the claims as follows.

Claims 1-12 (canceled).

13. (currently amended) A trench flash memory device, comprising:

a substrate having a trench;

a gate structure, which is located in the trench, comprising ~~and has the following components from outside to inside of the trench:~~ a tunnel oxide layer, a floating gate over the tunnel oxide layer, a gate dielectric layer over the floating gate and a control gate over the gate dielectric layer, wherein the tunnel oxide layer, the floating gate and the gate dielectric layer wrap around a bottom portion of the control gate;

a source region, ~~which is~~ located in the substrate around the bottom of the trench; and

a drain region, ~~which is~~ located in the substrate adjacent to the top of the trench.

4. **14. (currently amended) The device of claim 13, further comprising:**

a first well region ~~having~~ of a first ~~conduction~~ conductive type, formed in the substrate and connected with the source region;

a second well region ~~having~~ of a second ~~conduction~~ conductive type, formed above the first well region; and

a third well region ~~having~~ of the first ~~conduction~~ conductive type formed in the substrate, which connects the second well region with the first well region.

15. (original) The device of claim 14, wherein the first well region having the first conduction type includes a deep n-type well region.

16. (original) The device of claim 14, wherein the second well region having the second conduction type includes a p-type well region.

17. (original) The device of claim 14, wherein the third well region having the first conduction type includes an n-type well region.

18. (original) The device of claim 13, wherein the gate dielectric layer includes silicon oxide/silicon nitride/silicon oxide layer.

19. (original) The device of claim 13, wherein the floating gate has a top surface lower than the upper surface of the substrate.

20. (original) The device of claim 13, wherein the control gate has a top surface higher than the upper surface of the substrate.

21. (new) A trench flash memory device, comprising:

a substrate having a trench;

a gate structure, located in the trench, comprising a tunnel oxide layer disposed conformal to the trench, a floating gate disposed over the tunnel oxide layer, a gate dielectric layer disposed over the floating gate and a control gate disposed over the gate dielectric layer, wherein the tunnel oxide layer, the floating gate and the gate dielectric layer surround a bottom portion of the control gate;

a first doped region, located in the substrate around a bottom of the trench; and

a second doped region, located in the substrate adjacent to a top of the trench.

22. (new) The device of claim 21, further comprising:

a first well region of a first conductive type, formed in the substrate and connected with the source region;

a second well region of a second conductive type, formed above the first well region; and

a third well region of the first conductive type, formed in the substrate, which connects the second well region with the first well region.

23. (new) The device of claim 21, wherein the first doped region is a source region and the second doped region is a drain region.

24. (new) The device of claim 22, wherein the third well region having the first conduction type includes an n-type well region.

25. (new) The device of claim 21, wherein the gate dielectric layer includes silicon oxide/silicon nitride/silicon oxide layer.

26. (new) The device of claim 21, wherein the floating gate has a top surface lower than the upper surface of the substrate.

27. (new) The device of claim 21, wherein the control gate has a top surface higher than the upper surface of the substrate.

28. (new) A trench flash memory device, comprising:

a substrate having a trench; and

a gate structure, located in the trench, comprising a tunnel oxide layer disposed conformal to the trench, a floating gate disposed over the tunnel oxide layer, a gate dielectric layer disposed over the floating gate and a control gate

disposed over the gate dielectric layer, wherein the tunnel oxide layer, the floating gate and the gate dielectric layer surround a bottom portion of the control gate;

a source region, located in the substrate around the bottom of the trench;

a drain region, located in the substrate adjacent to the top of the trench;

a first well region of a first conductive type, formed in the substrate and connected with the source region;

a second well region of a second conductive type, formed above the first well region; and

a third well region of the first conductive type, formed in the substrate, which connects the second well region with the first well region.

29. (new) The device of claim 28, wherein the third well region having the first conduction type includes an n-type well region.

30. (new) The device of claim 28, wherein the gate dielectric layer includes silicon oxide/silicon nitride/silicon oxide layer.

31. (new) The device of claim 28, wherein the floating gate has a top surface lower than the upper surface of the substrate.

32. (new) The device of claim 28, wherein the control gate has a top surface higher than the upper surface of the substrate.